

NOTE: This disposition is nonprecedential.

**United States Court of Appeals
for the Federal Circuit**

**MICRON TECHNOLOGY, INC., MICRON
SEMICONDUCTOR PRODUCTS, INC., MICRON
TECHNOLOGY TEXAS, LLC,**
Appellants

v.

BESANG INC.,
Appellee

2025-1320

Appeal from the United States Patent and Trademark
Office, Patent Trial and Appeal Board in No. IPR2023-
00900.

INTEL CORPORATION,
Appellant

v.

BESANG INC.,
Appellee

2025-1377

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2023-00991.

Decided: October 30, 2026

XIN-YI ZHOU, O'Melveny & Myers LLP, Los Angeles, CA, argued for Micron Semiconductor Products, Inc., Micron Technology Texas, LLC and Micron Technology, Inc. Also represented by BENJAMIN HABER; WILLIAM FINK, KHANH NGUYEN LEON, Washington, DC; JOHN C. KAPPOS, Dallas, TX.

TYLER R. BOWEN, Ashurst Perkins Coie US LLP, Phoenix, AZ, argued for Intel Corporation. Also represented by ANDREW DUFRESNE, Madison, WI; JESSICA KAISER, Denver, CO; MATTHEW A. LEMBO, New York, NY.

MICHELLE ARMOND, Armond Wilson LLP, Newport Beach, CA, argued for BeSang Inc. Also represented by JOSEPH LI; DOUGLAS R. WILSON, Austin, TX.

Before LOURIE, REYNA, and HUGHES, *Circuit Judges*.

LOURIE, *Circuit Judge*.

Appellants Micron Technology Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC (collectively, “Micron”) and Intel Corporation (“Intel”) separately appeal from two *inter partes* review (“IPR”) final written decisions of the United States Patent Trial and Appeal Board (“the Board”) determining that claims 1 and 13–17 of BeSang Inc.’s (“BeSang’s”) U.S. Patent 7,378,702 (“the ’702 patent”) were not

unpatentable. See *Micron Tech., Inc. v. BeSang Inc.*, No. IPR2023-00900, 2024 WL 4765857 (P.T.A.B. Nov. 13, 2024) (“*Micron Decision*”); *Intel Corp. v. BeSang Inc.*, No. IPR2023-00991, 2024 WL 5076376 (P.T.A.B. Dec. 11, 2024) (“*Intel Decision*”). For the following reasons, we affirm.

BACKGROUND

The ’702 patent is directed to “the use of ‘a plurality of vertically oriented semiconductor memory devices, or cells,’ that ‘may be added to a separately fabricated substrate that includes electrical devices and/or interconnect lines.’” *Micron Decision*, 2024 WL 4765857, at *1 (citing ’702 patent col. 1 ll. 40–50). The goal of the invention is to reduce the lateral area of transistors on a chip. *Id.*

Claims 1 and 13 of the ’702 patent, representative for this appeal, read as follows:

1. A semiconductor memory structure, comprising:

a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and

a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells *separated from each other by dielectric material*;

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as

measured from the bottom surface of the substrate; and

wherein the memory cell is a DRAM having at least one transistor.

13. A semiconductor memory structure, comprising:

a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;

a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and

the stackable add-on layer being bonded to the dielectric layer; and

wherein the memory cells are nonvolatile memory cells having at least one transistor.

'702 patent, col. 10 ll. 47–63; *id.* at col. 12 ll. 24–34 (emphases added).

Micron and Intel each petitioned for IPR, alleging that claims of the '702 patent would have been obvious over the prior art at the time of the invention. *See Micron Decision*, 2024 WL 4765857, at *1; *Intel Decision*, 2024 WL 5076376, at *1. Both parties challenged claims 13–17 of the '702 patent; Intel additionally challenged claim 1. *See Micron Decision*, 2024 WL 4765857, at *1; *Intel Decision*, 2024 WL 5076376, at *1. The Board instituted both IPRs. *See Micron Decision*, 2024 WL 4765857, at *1; *Intel Decision*, 2024 WL 5076376, at *1.

In the *Micron Decision*, the Board determined that Micron did not meet its burden to show that claim 13 would have been obvious over U.S. Patent 5,091,762

(“Watanabe”) or a combination of Watanabe and U.S. Patent 6,881,994 (“the Lee Patent”) because (1) the petition was not directed to “nonvolatile memory cells,” as required by the claim; (2) Watanabe was not enabled as prior art; and (3) a skilled artisan would not have been motivated to combine Watanabe with the Lee Patent. *Micron Decision*, 2024 WL 4765857, at *11–12 (nonvolatile memory analysis); *id.* at *13–15 (enablement analysis); *id.* at *17–18 (combination analysis).

In the *Intel Decision*, the Board determined that Intel did not meet its burden to show that claims 1 and 13 were unpatentable. Regarding claim 1, the Board rejected Intel’s argument that the claim would have been obvious over U.S. Patent Application 2003/0157748 A1 (“Kim”) and U.S. Patent 5,571,730 (“Park”) because the combination did not disclose “memory cells [] separated from each other by dielectric material.” *Intel Decision*, 2024 WL 5076376, at *24–25. Regarding claim 13, the Board determined that Intel did not meet its burden to show that the claim would have been obvious over (1) U.S. Patent Application 2002/0028541 A1 (“the Lee Application”); (2) the combination of Lee and an article on a thin film transfer process (“Aspar”); and (3) the combination of the Lee Application and Kim. *Id.* at *7–8 (Lee Application analysis); *id.* at *9–15 (Lee Application and Aspar analysis); *id.* at *16–20 (Lee Application and Kim analysis). For all three rejections, the Board determined that Intel did not meet its burden because it did not demonstrate that the Lee Application taught limitation 13[b], that is, “a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells.” *Id.* at *7–8 & nn. 9, 15.

Micron and Intel separately and timely appealed. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

While both appeals concern the ’702 patent, the grounds for challenging the relevant claims in each appeal

differ. *See Micron Decision*, 2024 WL 4765857, at *3; *Intel Decision*, 2024 WL 5076376, at *3. Accordingly, we address each appeal separately.

I

Beginning with Micron’s appeal, we evaluate the Board’s determination that Micron did not meet its burden to show that claim 13 would have been obvious over Watanabe or the combination of Watanabe and the Lee Patent.

A

We first address the ground involving only Watanabe—*i.e.*, the Board’s determination that Watanabe was not enabled prior art. *See Micron Decision*, 2024 WL 4765857, at *12–15. “In the absence of such other supporting evidence to enable a skilled artisan to make the claimed invention, a standalone § 103 reference must enable the portions of its disclosure being relied upon.” *Raytheon Techs. Corp. v. Gen. Elec. Co.*, 993 F.3d 1374, 1381 (Fed. Cir. 2021). “In this context the reference must necessarily enable the relied-upon portion of *its own disclosure*.” *Id.* (emphasis added).

“Whether a prior art reference is enabling is a question of law based upon underlying factual findings.” *Id.* (internal quotation marks and citation omitted). “We review the Board’s legal conclusions *de novo* and its underlying factual determinations for substantial evidence.” *Id.* Substantial evidence is “such relevant evidence as a reasonable mind might accept as adequate to support a conclusion.” *Consol. Edison Co. of N.Y. v. NLRB*, 305 U.S. 197, 229 (1938).

The Board concluded that Watanabe was not enabled because it disclosed bonding its stacked layers using a thermal process at 900–1000°C, but such a temperature would severely impact its structure and risk destroying the underlying electronic components in its substrate. *Micron Decision*, 2024 WL 4765857, at *14–15. That

conclusion was supported by substantial evidence in the form of the expert testimony that such a temperature as disclosed in Watanabe would risk destroying the electronic components on the substrate, Micron J.A. 3632–34 (Micron’s expert testifying that a bonding temperature over 650°C would risk destroying underlying electronic components); Micron J.A. 3757–58 (BeSang’s expert declaration stating the same), and thus would not allow a skilled artisan to make and use the invention, *see Raytheon*, 993 F.3d at 1380.

Micron’s counterarguments are unpersuasive. It first argues that the Board implicitly construed claim 13 by importing a temperature requirement—that the processing temperature in the claimed structure could not exceed 650°C—from the specification into the claims. *See* Micron Open. Br. 22. The Board made no such construction. Rather, the Board made a factual finding: It relied on expert testimony stating that temperature processing of Watanabe’s structure could not exceed 650°C without damaging/destroying its electronic components, *see* Micron J.A. 3632, such that Watanabe’s processing at 900–1000°C was not enabled, *see Micron Decision*, 2024 WL 4765857, at *14–15. Such a determination was not a claim construction because the Board did not “establish[] the scope . . . and meaning of the patented subject matter.” *See Google LLC v. EcoFactor, Inc.*, 92 F.4th 1049, 1055 (Fed. Cir. 2024) (emphasis omitted). Rather, the Board concluded that, in view of expert testimony, Watanabe was not enabled because its temperature processing did not enable a skilled artisan to make or use its invention. That is a conclusion on enablement, not claim construction, and the factual findings underlying that conclusion were supported by substantial evidence.

Micron next argues that other evidence renders Watanabe enabled for purposes of the claim 13 obviousness analysis. Micron relies on evidence of a so-called “thermal budget”—*i.e.*, consideration of both time and temperature,

not just temperature—and argues that a skilled artisan would understand that 900–1000°C temperature bonding could occur for a short time. *See* Micron Open. Br. 37–43. But the Board considered such evidence and rejected it in light of the expert testimony above. *See Micron Decision*, 2024 WL 4765857, at *13–15. As explained above, that expert testimony constitutes substantial evidence.

Because Micron relied solely on Watanabe for this obviousness ground, the Board’s conclusion was supported by substantial evidence. Micron points us to no other evidence that would enable a skilled artisan to make the claimed invention, so that ground must fail. *See Raytheon*, 993 F.3d at 1377 (“We have also previously expounded the principle that if an obviousness case is based on a non-self-enabled reference, and no other prior art reference or evidence would have enabled a skilled artisan to make the claimed invention, then the invention cannot be said to have been obvious.”).

B

Moving beyond the Watanabe-only ground, Micron argues that the Board erred in rejecting Micron’s obviousness arguments by determining that there was no motivation to combine Watanabe and the Lee Patent. Micron Open. Br. 58–61.

In its analysis, the Board rejected Micron’s argument that combining the Lee Patent’s device with Watanabe’s stacking method would result in benefits to the device. *Micron Decision*, 2024 WL 4765857, at *17–18. It reasoned that Micron did not sufficiently explain how such improvement would work and that any benefits would be outweighed by the damage to the Lee Patent’s device caused by Watanabe’s bonding temperature of 900–1000°C. *Id.*

The Board’s conclusion was supported by substantial evidence in the form of the same expert testimony that stated that a temperature of 900–1000°C would damage

the electronic devices in an underlying substrate. *See* Micron J.A. 3632; Micron J.A. 3757. That conclusion applies equally to the device of the Lee Patent. *See Micron Decision*, 2024 WL 4765857, at *18. Micron repeats the same arguments regarding the thermal budget—those arguments thus fail for the same reasons given above.

Micron also argues that the Board erred by improperly requiring Micron to show a specific improvement in the proposed combination. *See* Micron Open. Br. 60–61. We disagree with Micron’s interpretation of the Board’s decision. The Board specifically stated that “[i]n general, a petitioner need not demonstrate that a particular alternate method would improve a prior art device in order to show a motivation to combine.” *Micron Decision*, 2024 WL 4765857, at *18 (citing *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380–81 (Fed. Cir. 2023)). The Board therefore did not *require* that Micron show a specific improvement; rather, it specifically disposed of Micron’s argument that “affirmatively invoke[d] improvement of [the] Lee[] [Patent’s] device as a reason for the combination.” *See id.*; Micron J.A. 276–77 (Micron’s petition advancing said argument).

We accordingly conclude that the Board’s analysis of motivation to combine was supported by substantial evidence.¹

¹ Because we affirm on the Board’s Watanabe enablement and motivation to combine findings, we do not address Micron’s argument regarding nonvolatile memory. *See* Open. Br. 47–54; *Micron Decision*, 2024 WL 4765857, at *11 (describing the findings on enablement and nonvolatile memory cells as “separate and independent reasons” to reject Micron’s unpatentability arguments).

II

Next we consider Intel’s appeal. The Board determined that Intel did not meet its burden to show that claim 13 was unpatentable over the Lee Application, the combination of the Lee Application and Aspar, and the combination of the Lee Application and Kim. *Intel Decision*, 2024 WL 5076376, at *7–20. The Board also determined that Intel did not meet its burden to show that claim 1 was unpatentable over Park & Kim. *Id.* at *24–25. We analyze claim 13 and claim 1 in turn.

A

The Board determined that Intel failed to show that a skilled artisan would understand that the Lee Application taught limitation 13[b]—“a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells.” *Intel Decision*, 2024 WL 5076376, at *7–8. Intel does not appeal that determination, so any argument with respect to that factual finding is thus waived. *See Bozeman Fin. LLC v. Fed. Rsrv. Bank of Atlanta*, 955 F.3d 971, 974 (Fed. Cir. 2020).

Rather, Intel argues that it addressed the term “stackable add-on layer” from limitation 13[b] in its arguments with respect to limitation 13[c] (which contains the same claim term). *See Intel Open. Br.* 73–76. In Intel’s view, the Board abused its discretion by failing to consider such arguments with respect to its combination grounds for limitation 13[c] in its determination regarding limitation 13[b]. *See id.*

But Intel’s argument fails because it *explicitly relied on only the Lee Application* for limitation 13[b]. In its petition, Intel cross-referenced its argument regarding the Lee Application and limitation 13[b], stating that “for th[ose] same reasons . . . Lee discloses or suggests . . . 13[b].” Intel J.A. 177 (Lee Application and Kim); Intel J.A. 183 (Lee Application and Aspar). It then moved on to its limitation

13[c] argument, separating the two by a subheader indicating that the arguments for the two limitations were different. *See Intel J.A.* 177, 183. The Board thus did not abuse its discretion in interpreting the petition’s arguments regarding limitation 13[b]—that is, in considering only the arguments offered under the “13[b]” subheading in the petition in determining that Intel failed to show that the prior art renders that limitation obvious. *See Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023) (“The Board is entitled to discretion in how it interprets petitions.”).

Because the Board did not abuse its discretion, Intel’s waiver of arguments on the merits with respect to limitation 13[b] suffices to dispose of the argument regarding claim 13. The Board’s rejection of Intel’s reliance on the Lee Application for limitation 13[b] means that, on the record before us, Intel cannot demonstrate that a skilled artisan would have understood its proposed combinations to teach the claim limitation; its obviousness argument must fail.²

B

We finally address the Board’s determination that Intel failed to meet its burden to show that claim 1 would have been obvious over the combination of Park and Kim.

Before the Board, the parties’ dispute centered around the claim term “memory cells . . . *separated from each other by dielectric material.*” *Intel Decision*, 2024 WL 5076376, at *24 (emphasis added). The Board determined that there was no such separation in Park because its memory cells

² Because the Board’s determination that the Lee Application does not teach limitation 13[b] was not appealed, we do not reach the merits of Intel’s arguments regarding the combination of the Lee Application and Aspar or the Lee Application and Kim.

“share[d] [a] plate electrode . . . and gate electrode,” with only “some dielectric material between the memory cells.” *Id.* at *25. As such, the Board concluded that “the presence of some dielectric material between the memory cells, but not enough to electrically separate the cells from each other, [did] not meet the claim.” *Id.*

The Board’s conclusion was supported by substantial evidence in the form of Park’s figures 8 and 9, which show that adjoining memory cells share a plate and gate electrode with some dielectric material between the cells. *See* Intel J.A. 2099–2100. Intel does not dispute that factual finding on appeal. Rather, it argues that the Board implicitly construed claim 1 such that the term “separate from each other by dielectric material” required “electrical separation.” Intel Open. Br. 64–66. That argument is unpersuasive. Indeed, Intel itself argued that a skilled artisan would seek electrical separation because one would understand “the need to separate the memory cells with dielectric material for proper operation (*e.g., avoiding shorts*).” Intel J.A. 216 (emphasis added). It further argued that Park’s memory cells must be “*electrically separated*, as necessary for proper operations.” Intel J.A. 554 (emphasis added). The Board did not engage in an implicit claim construction, but instead disposed of Intel’s argument by comparing Park’s memory cells to the text of the claim, determining that the proposed combination did not have the necessary separation required by claim 1.

CONCLUSION

We have considered Micron’s and Intel’s remaining arguments but find them unpersuasive. For the foregoing reasons, we *affirm* the Board’s decisions. The respective claims were not shown to have been unpatentable.

AFFIRMED