United States Court of Appeals for the Federal Circuit

NETLIST, INC.,
Appellant

v.

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS, LLC,
Appellees

2024-1707

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2022-00639, IPR2023-00204.

Decided: September 2, 2026

JENNIFER ELIZABETH FISCHELL, MoloLamken LLP, Washington, DC, argued for appellant. Also represented by KAYVON GHAYOUMI, RAYINER HASHEM, JEFFREY A. LAMKEN, LIDIYA MISHCHENKO; ELIZABETH KATHLEEN CLARKE, Chicago, IL; CATHERINE MARTINEZ, New York, NY; JASON SHEASBY, HONG ANNITA ZHONG, Irell & Manella LLP, Los Angeles, CA; BLAIR A. SILVER, Washington, DC.

MICHAEL RUECKHEIM, King & Spalding LLP, San

Francisco, CA, for appellees. Also represented by JUAN C. YAQUIAN, Houston, TX.

Before REYNA, LINN, and STARK, *Circuit Judges*.

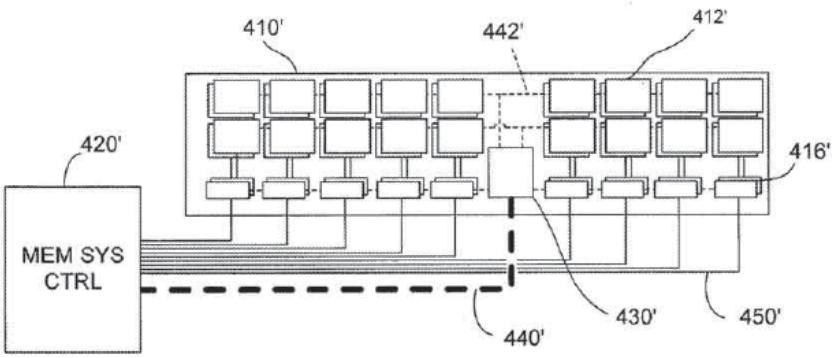
REYNA, *Circuit Judge*.

Netlist, Inc. ("Netlist") appeals a final written decision of the Patent Trial and Appeal Board ("Board") determining all challenged claims of U.S. Patent No. 10,949,339 are unpatentable as obvious. For the following reasons, we affirm.

BACKGROUND

Netlist owns U.S. Patent No. 10,949,339 (the "'339 patent"). The '339 patent is directed to computer memory systems, and more specifically to "improving the performance and the memory capacity of . . . memory boards that include dual in-line memory modules." J.A. 109 at 1:18–23. The specification describes adding to memory modules a plurality of "buffers" between a memory controller and dynamic random access memory ("DRAM") devices. The buffers include data paths that are ordinarily disabled, thereby electrically isolating the DRAM devices from the memory controller by default. During read or write operations, however, the buffers are selectively enabled to "drive[] the data signal" from the memory controller to the DRAM devices. J.A. 117 at 17:14–22.

Figure 3C of the '339 patent, reproduced below, depicts one embodiment of the invention. In that embodiment, buffer circuits 416′ are "operatively coupled" between memory controller 420′ and memory devices 412′.



J.A. 104 at Fig. 3C.

Samsung Electronics Co., Ltd. ("Samsung") filed a petition for *inter partes* review challenging claims 1–35 of the '339 patent as obvious over the combination of U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"; J.A. 1831–56) and U.S. Patent No. 7,024,518 ("Halbert"; J.A. 1857–76).[1] The Board treated independent claim 1 of the '339 patent as representative in its final written decision. The parties do the same on appeal, as do we in our

[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC (collectively, "Micron") filed a petition for *inter partes* review in IPR2023-00204 challenging the same claims over the same prior art and were joined as petitioners with Samsung in IPR2022-00639. Although Samsung and Micron were both originally parties to this appeal, Samsung has since settled with Netlist and withdrawn its participation from this appeal. We therefore refer to Micron alone as "Appellees."

review. Claim 1, reproduced below, recites a memory module having various components.

> [1pre] A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:
>
> [1a] a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket;
>
> [1b] double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks;
>
> [1c1] a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals,
>
> [1c2] wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control

signals in response to at least some of the input address and control signals; and

[1d1] a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals,

[1d2] wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side,

[1d3] wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;

[1e] wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period; and

[1f] wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wise write data to the respective module data lines during the first time period.

J.A. 118 at 19:9–67.

Two limitations of claim 1 are disputed on appeal. First, limitations [1e] and [1f] require that a "data path" through the buffer is "enabled" so that a memory controller can drive write data through the buffer to the DRAM device. Second, limitation [1e] separately requires that the data path is enabled at a certain time (i.e., "in accordance with a latency parameter") for a certain duration (i.e., a "first time period").

The Board instituted review and determined that Samsung established by a preponderance of the evidence that all challenged claims of the '339 patent were obvious over Ellsberry and/or Halbert. The Board found that "Ellsberry alone or in combination with Halbert, when viewed with the general knowledge of a person of ordinary skill in the art, teaches enabling and disabling data paths through the data buffer." J.A. 42. The Board further found that Appellees "established that Ellsberry's switch ASICs use Posted CAS latency (AL) bits to control timing of the enablement of the data path across its switch ASICs," i.e., that enablement of the buffer data path occurs for a first time period in accordance with a latency parameter. J.A. 47.

Netlist appealed from the Board's final written decision. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

STANDARD OF REVIEW

We review the Board's ultimate obviousness determination de novo and its underlying factual findings for substantial evidence. *Incept LLC v. Palette Life Scis., Inc.*, 77 F.4th 1366, 1371 (Fed. Cir. 2023). Substantial evidence is "such relevant evidence as a reasonable mind might accept as adequate to support a conclusion. *Id.* (citation modified).

We review de novo the Board's compliance with its obligations under the Administrative Procedure Act ("APA"), 5 U.S.C. § 706. *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th

1374, 1380 (Fed. Cir. 2023). The APA requires the Board to identify the reasons and bases in the record for reaching its conclusions. *Alacritech, Inc. v. Intel Corp.*, 966 F.3d 1367, 1370 (Fed. Cir. 2020). "We do not require perfect explanations, and we will uphold a decision of less than ideal clarity if the agency's path may reasonably be discerned." *Id.* (citation modified).

An *inter partes* review must proceed "in accordance with or in conformance to the petition." *SAS Inst., Inc. v. Iancu*, 584 U.S. 357, 365 (2018) (citation modified). The Board may not "depart from the petition and institute a *different* inter partes review of [its] own design." *Id.* (emphasis in original); *see also id.* at 364 ("[R]ather than create (another) agency-led, inquisitorial process for reconsidering patents, Congress opted for a party-directed, adversarial process."). Thus, we have found error where the Board held claims unpatentable based on a ground "absent from the petition." *Int'l Bus. Machs. Corp. v. Zillow Grp, Inc.*, 160 F.4th 1360, 1366 (Fed. Cir. 2025) (citing *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020)).

DISCUSSION

Netlist makes two primary arguments on appeal. First, Netlist argues that the Board erred by determining that Ellsberry teaches data paths that are enabled "in accordance with a latency parameter," as recited in limitation [1e]. Appellant Br. 37–51. Second, Netlist argues the Board erred by determining that Ellsberry teaches "enabl[ing]" a "data path," as recited by limitations [1e] and [1f]. *Id.* at 51–62. We address each argument in turn. Additionally, Netlist raises various other APA related arguments which we address below.

I.

Netlist argues the Board erred by finding that Ellsberry teaches data paths that are enabled at the required

time using a latency parameter, as required by limitation [1e]. Netlist argues the Board's finding that Ellsberry teaches buffers, i.e., "switch ASICs," that use a latency parameter, i.e., "Posted CAS_n," to control timing of enabling the buffer data paths, was based on "unsubstantiated speculation about Ellsberry's operation." Appellant Br. 38–39. Netlist contends that the Board merely assumed that Ellsberry's switch ASICs use the Posted CAS_n command to control enabling data paths. More specifically, Netlist argues that, in Ellsberry, Posted CAS_n is simply passed through the switch ASIC to the DRAM devices instead of being used by the switch ASICs. We are unpersuaded by Netlist's arguments and determine that the Board's finding was supported by substantial evidence.

The Board, relying on the opinion of Samsung's expert, Dr. Subramanian, found that Ellsberry teaches certain memory module embodiments having a control unit that controls switch ASICs to enable or disable data paths, i.e., Ellsberry's Ports A and B.[2] J.A. 40 (citing Ellsberry, Figs. 2, 4, ¶¶30–31, 40; Subramanian Decl. [J.A. 1302–1830], ¶¶231, 358). And as to enabling the data paths in accordance with a latency parameter, the Board pointed to Ellsberry's teaching that initialization commands, including a "Posted CAS_n parameter," are sent to and stored in Ellsberry's memory bank switch (i.e., switch ASIC). J.A. 44 (citing Ellsberry, ¶44, Fig. 9). The Board rejected Netlist's argument that Ellsberry's memory bank switch "merely passes the Posted CAS_n latency parameter (AL) to the memory devices along with the burst length (BL) and CAS latency parameter (CL)," because, of those three parameters, Ellsberry's Paragraph 44 refers

---

[2] Netlist also argues that the Board erred by finding enablement of Ellsberry's Ports A and B constitutes enablement of the claimed "data paths." We address that contention in Section II below.

specifically to storing Posted CAS_n in the memory bank switch. *Id.* Paragraph 44 discloses that certain commands are sent to Ellsberry's memory bank switch instead of being passed directly to the memory devices, including those shown in Figure 9, i.e., Posted CAS_n. Ellsberry, ¶44, Fig. 9.

The Board then turned to Ellsberry's disclosure that its memory modules are compatible with Joint Electron Device Engineering Council ("JEDEC") standards. J.A. 44 (citing Ellsberry, ¶¶27, 44, 50, Fig. 9). And specifically, that Figure 21 from the JEDEC standards provides read and write latencies that depend upon "Posted CAS latency (or additive latency)." J.A. 45 (citing J.A. 2130; Subramanian Decl., ¶352). The Board's reliance on Ellsberry's teachings, as supported by the JEDEC standards, constitutes substantial evidence that Ellsberry teaches enabling data paths in accordance with a latency parameter.

Netlist further argues that, even if the Board had substantial evidence to find that Ellsberry uses latency information to control data paths, the Board erred by using the '537 patent,[3] which was not part of Samsung's petition ground, to supply the missing limitation of enabling the data paths at the required time to account for the buffer. Netlist argues that Ellsberry's "'Posted CAS_n,' the Petition's putative latency parameter, did not reflect timing information for the module and had nothing to do with a data buffer." *Id.* at 44–45 (emphasis omitted). Thus, Netlist argues, the Board improperly used Netlist's own '537 patent to fill that limitation gap.

Samsung did not assert the '537 patent as a reference in its sole petition ground. Yet the Board relied on the '537

---

[3] The '537 patent refers to U.S. Patent No. 7,532,537 (J.A. 2531–78) which issued May 12, 2009 and is assigned to Netlist.

patent's "*teaching*" of "add[ing] one clock cycle to account for propagation delay through a data buffer." J.A. 46 (emphasis added) (citing '537 patent at 21:28–53). The Board continued that, "[p]rimed with this teaching, a person of ordinary skill in the art would have implemented Ellsberry to budget one clock cycle to account for delay through the data buffer." *Id.* According to Netlist, the Board's explanation shows that it impermissibly expanded the role of the '537 patent from mere evidence of the general skill in the art to that of a prior art reference. This would violate the restriction that the Board may not depart from the petition and find claims invalid on grounds "of [its] own design." *SAS Inst.*, 584 U.S. at 365; *see also Koninklijke Philips*, 948 F.3d at 1335 (noting that the Board may not rely on a "combination of prior art references not advanced in . . . [the] petition"). Netlist further contends that even if the Board had not elevated the role of the '537 patent to a prior art reference, and instead had used it merely as evidence of general knowledge in the art, the Board's treatment of the '537 patent was still improper.

However, any potential error was harmless because the Board alternatively found that Ellsberry alone, without relying on the '537 patent, teaches adding one clock cycle to account for propagation delay through its switch ASICs. The Board pointed to Samsung's argument that the Posted CAS latency accounts for the time needed for data to traverse a buffer, i.e., one clock cycle. And it cited Dr. Subramanian's deposition testimony that Ellsberry's note under Figure 8B—"if cl_mode. = subtract; cl = cl – 1 to DDRs"—would have been understood "as meaning that one cycle has been added to account for propagation delay through the data buffer" so that "one cycle should be subtracted from the overall latency so that the system memory controller encounters the same delay it would have in the absence of the data buffer." J.A. 46 (citing Subramanian Dep. Tr. [J.A. 9000–356] at 182:16–22). The Board's determination that Ellsberry teaches that Posted CAS_n adds

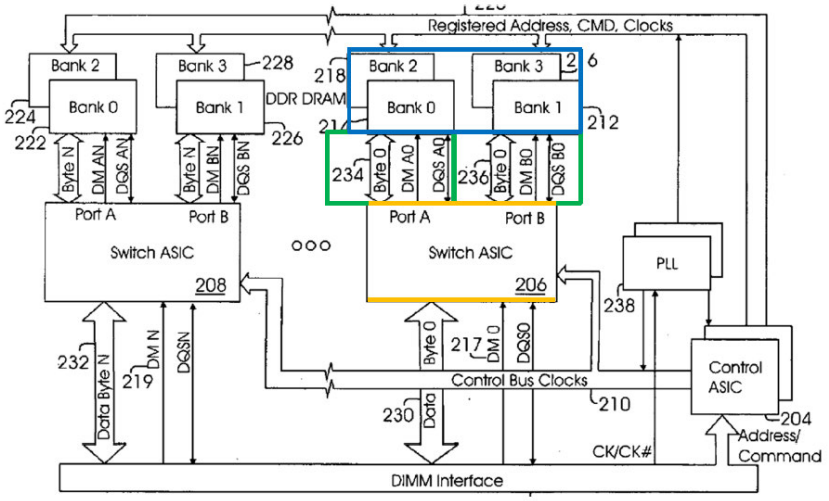
one clock cycle of latency to account for the buffers is supported by substantial evidence and comports with the ground presented in the petition. Thus, we need not consider whether the Board improperly relied on the '537 patent.

II.

Netlist argues the Board erred by determining that Ellsberry teaches "enabl[ing]" a "data path," as recited by limitations [1e] and [1f]. Appellant Br. 51–62. Those limitations require that, during a write operation, the buffer's data path is enabled to drive data from the memory controller to the DRAM devices. Netlist argues those limitations require "***connecting*** and ***disconnecting*** data paths" within the buffer "to isolate DRAM devices." Appellant Br. 52. Netlist argues that Ellsberry operates differently. Specifically, that Ellsberry's switch ASIC "merely ***selects*** a memory bank to receive data" by "enabling and disabling ***memory banks***—located outside the buffer—using commands and signals directed to the memory banks themselves" instead of "connecting and disconnecting ***data paths*** in the buffer to isolate DRAM devices." *Id.* (emphases in original). We disagree.

Netlist challenges the Board's finding that paragraph 31 of Ellsberry teaches this limitation. Specifically, the Board relied on Ellsberry's teaching that the switch ASIC, which the Board mapped to the claimed buffer, "caus[es] Port B to be activated and Port A to be disabled." Appellant Br. 52 (citing J.A. 40 (quoting Ellsberry, ¶ 31)). Netlist argues this paragraph does not teach enabling the claimed "data path" because Ports A and B that it refers to are located *outside of the switch ASIC* (i.e., the claimed buffer) instead of *within the switch ASIC*, as required by the claims.

Netlist's only support for this argument derives from its annotated version of Ellsberry's Figure 2 reproduced below. What Netlist added to Figure 2 are the colored blue, green, and yellow boxes. Netlist argues that the green boxed area, which it drew outside of switch ASIC 206, shows the location of Ports A and B. Therefore, Netlist argues, Ports A and B cannot be the same thing as the claimed data paths, which must be within the yellow boxed area. Netlist also argues that Ellsberry does not truly enable "ports," but instead "refers to enabling and disabling ***memory banks*** associated with the ports." Appellant Br. 53; *see also id.* at 59–62. Memory banks 216 and 218 in Figure 2 are outlined in blue, and also fall outside the yellow boxed area.



Appellant Br. 53 (Ellsberry, Fig. 2 (annotated)).

The Board considered and rejected Netlist's arguments as "manifestly incorrect." J.A. 71. The Board found that "Ellsberry clearly shows Ports A and B as parts of the switch ASICs, not the physical memory banks." *Id.* As shown above, Ports A and B are depicted as components inside of Netlist's own yellow boxed area. Moreover, Ellsberry teaches that "memory bank switch 206 *includes*

Port A and Port B, coupled to data buses 234 & 236 respectively." Ellsberry, ¶ 30 (emphasis added). And the Board further found that Ellsberry's disclosure in paragraph 31 of disabling the ports means disabling data paths through the switch ASIC, not disabling the memory banks themselves. J.A. 72. The Board's finding aligns with Figure 2, which shows that the memory banks 216 and 218 are separate components from Ports A and B. We therefore conclude that the Board's reliance on Ellsberry's paragraph 31 and associated Figure 2 constitutes substantial evidence that Ellsberry teaches enabling ports within the claimed buffer.

Netlist next challenges the Board's finding that Ellsberry's teaching of enabling "ports" correlates to enabling "data paths." Netlist argues that data paths and ports are separate components and can be controlled independently. Netlist argues both that the Board's finding that "enabling a port means that the data path through the port is enabled" is unsupported by substantial evidence and that its failure to explain its reasoning violates the APA. Appellant Br. 54–55 (citing J.A. 70). We disagree.

The Board gleaned from Figure 4 of Ellsberry that "the only elements within the data processing unit 400 (part of the switch ASIC) that the data paths pass through are bidirectional drivers 402, 404." J.A. 40. The Board further found, relying on the testimony of Dr. Subramanian, that "this would suggest to one of ordinary skill in the art that the bidirectional drivers 402, 404 are what enables or disables data paths," i.e., Ports A and B. J.A. 40–41; J.A. 40–42 (citing Subramanian Decl. ¶¶ 159, 239–40). We conclude that the Board's reasoning is sufficient under the APA and is supported by substantial evidence.

Netlist further argues that Ellsberry is silent as to whether its bidirectional drivers are even capable of enabling data paths. As we discuss above, the Board credited Dr. Subramanian's testimony that Ellsberry's bidirectional

drivers 402 and 404 enable data paths through the switch ASIC. We conclude this is substantial evidence that Ellsberry discloses enabling data paths.

Notably, Netlist ignores the Board's alternative determination that Ellsberry *in view of Halbert* teaches enabling data paths. The Board stated: "To the extent there is any doubt as to what in Ellsberry's memory bank switch performs these functions, there is no dispute that Halbert's bidirectional buffers 122 and bidirectional data registers 126 and 128 have the capability to enable and disable data paths because they are illustrated in Figure 4 as symbols recognized in the art as tristate buffers." J.A. 42. The Board further included several pages of discussion explaining the motivation to combine Halbert's tristate buffers with Ellsberry's bidirectional drivers. *See* J.A. 19–26. The Board's alternative determination that Ellsberry and Halbert teach enabling data paths is also supported by substantial evidence.

III.

Netlist raises several other issues with respect to the APA. First, Netlist includes a two-sentence argument that the Board violated the APA in addressing "most limitations of claim 1 and the vast majority of the challenged claims" by limiting its analysis to "summarizing Samsung's 'contentions' and finding that Netlist 'does not dispute' them." Appellant Br. 66–67 (citations omitted). But Netlist does not specify which limitations it challenges or provide any further substantive argument on this point. We therefore find that Netlist failed to properly raise this argument for our consideration. *See Monsanto Co. v. Scruggs*, 459 F.3d 1328, 1341 (Fed. Cir. 2006) ("In order for this court to reach the merits of an issue on appeal, it must be adequately developed.").

Netlist separately asserts that the Board's failure to address its arguments for dependent claims 7, 16, and 21 was in violation of its APA obligations. Specifically, Netlist

argues that remand is required for those claims because the Board did not address its arguments that the prior art fails to teach the claimed "module control signals." We disagree.

Dependent claim 7 recites that the module controller must "use the module control signals to control timing of the first time period in accordance with the latency parameter." J.A. 118 at 20:40–43. Dependent claims 16 and 21 are substantially similar. Netlist argued in two brief paragraphs in its Patent Owner Response that Samsung failed to demonstrate that the prior art meets these claims for two reasons. First, Netlist argued that Samsung failed to demonstrate that Ellsberry's latency parameter was "included as part of the signals sent on bank switch control 210." J.A. 8554. Second, Netlist argued that "there is no evidence that [Ellsberry's] latency parameter are [sic] ever used to control the operation of the switch ASICs." J.A. 8555.

The Board directly addressed both of Netlist's arguments for claims 7, 16, and 21 in its Final Written Decision. The Board rejected Netlists arguments, finding instead that Samsung had shown that Ellsberry teaches that "the Posted CAS_n (AL) latency parameter is sent to and stored in the switch ASICs using an EMRS command." J.A. 59. The Board also cited back to its prior discussion for limitation [1e]. *Id.* (citing J.A. 43–50). For limitation [1e], the Board pointed to and agreed with Samsung's contention that Ellsberry's latency parameters are "set during initialization" and then "every read and write operation is performed in accordance with those latency parameters." J.A. 43–44 (internal quotations omitted).

The term "module control signals" first appears in claim limitation [1c2]. The Board found Ellsberry met that limitation by teaching control signals passed along bus 210 output from Control ASIC 204 in response to the input address and control signals for a "write" operation. J.A. 34.

Putting the Board's findings for limitations [1c2], [1e], and claim 7 (and 16 and 21) together, the Board accepted that Ellsberry's control signals for a write operation are performed in accordance with a latency parameter by virtue of initialization programming. Claims 7, 16, and 21 do not require that the "module control signals" *include* the latency parameter, only that the signal controls "*in accordance with* the latency parameter." Thus, we conclude that the Board's determination that Ellsberry teaches dependent claims 7, 16, and 21 is supported by substantial evidence. And because we can discern the Board's path to reaching its conclusion for these claims, we conclude there is no APA violation. *Alacritech*, 966 F.3d at 1370–71.

CONCLUSION

We have considered Netlist's other arguments but do not find them persuasive. For these reasons, we affirm.

AFFIRMED

COSTS

Costs against Netlist.