United States Court of Appeals for the Federal Circuit

VLSI TECHNOLOGY LLC,
Plaintiff-Appellant

v.

INTEL CORPORATION,
Defendant-Appellee

2024-1772

Appeal from the United States District Court for the Northern District of California in No. 5:17-cv-05671-BLF, Judge Beth Labson Freeman.

Decided: April 14, 2026

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Before MOORE, *Chief Judge*, CHEN, *Circuit Judge*, and KLEEH, *Chief District Judge*.[1]

MOORE, *Chief Judge*.

VLSI Technology LLC (VLSI) appeals orders of the United States District Court for the Northern District of California (1) granting Intel Corporation's (Intel) motion for summary judgment of noninfringement of U.S. Patent No. 8,566,836 on two separate grounds and (2) striking the damages theories of one of VLSI's damages experts. For the following reasons, we reverse-in-part, affirm-in-part, and remand for further proceedings consistent with this opinion.

BACKGROUND

In 2017, VLSI sued Intel for infringement of eight patents, including the '836 patent at issue in this appeal. The '836 patent relates to choosing one or more cores of a multicore processor to execute a particular task, for example, based on whether the task must be executed on a single core or can be executed across multiple cores. *See* '836 patent at 1:56–2:13, 6:60–7:11. VLSI asserted infringement of claims 1, 9–11, 13, 17, and 20–21 of the '836 patent. J.A. 4. Claims 1 and 10 are respectively representative of the asserted method and apparatus claims.

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[1] Honorable Thomas S. Kleeh, Chief Judge, United States District Court for the Northern District of West Virginia, sitting by designation.

> Claim 1 reads:
>
> 1. A method for operating a multi-core processing device, comprising:
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> ***measuring*** a processing speed parameter for each of a plurality of cores;
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> storing each measured processing speed parameter for each of the plurality of cores in a storage device; and
>
> ***upon identifying*** a processing task that can not be run across the plurality of cores, ***selecting a core*** from the plurality of cores having a fastest measured processing speed parameter at a given voltage to run the processing task.

'836 patent at 10:44–54 (emphases added).

> Claim 10 reads:
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> 10. A multi-core system on chip (SOC), comprising:
>
> a plurality of cores, each core comprising ***a performance measurement circuit for measuring a performance parameter value for said core***; and
>
> at least a first storage device for storing the performance parameter values for the plurality of cores for use in ***selecting a core*** having maximized or minimized performance parameter value at a specified voltage ***to run a processing task that can not be run across the plurality of cores***.

Id. at 11:20–29 (emphases added).

Relevant to this appeal, the district court construed the claims and, during discovery, struck certain theories of VLSI's damages expert, Dr. Sullivan, because the court determined VLSI failed to adequately disclose those theories in its damages contentions. J.A. 74–101 (claim

construction order); J.A. 66–73 (order striking theories); J.A. 58–65 (order denying VLSI's motion for relief with respect to struck theories). The court then granted Intel summary judgment of noninfringement of all asserted claims of the '836 patent based on (1) extraterritoriality and (2) rejection of VLSI's doctrine of equivalents (DOE) theory of infringement. J.A. 3–57. VLSI appeals the grant of summary judgment on both grounds as well as the striking of Dr. Sullivan's damages theories. We have jurisdiction under 28 U.S.C. § 1295(a)(1).

DISCUSSION

I. Summary Judgment of Noninfringement

We review a district court's summary judgment rulings under the law of the regional circuit, here the Ninth Circuit. *Adasa Inc. v. Avery Dennison Corp.*, 55 F.4th 900, 907 (Fed. Cir. 2022) (applying Ninth Circuit law). "The Ninth Circuit 'review[s] the district court's grant of summary judgment de novo, determining whether, viewing all evidence in the light most favorable to the nonmoving party, there are any genuine issues of material fact and whether the district court correctly applied the relevant substantive law.'" *Id.* (quoting *Kraus v. Presidio Tr. Facilities Div./Residential Mgmt. Branch*, 572 F.3d 1039, 1043–44 (9th Cir. 2009)). We first address VLSI's summary judgment arguments with respect to extraterritoriality and then VLSI's arguments relating to its DOE theory.

A. Extraterritoriality

1. The Asserted Method Claims

VLSI argues the district court erred in granting summary judgment of noninfringement of the asserted method claims because the court concluded there was no genuine dispute that the claims' measurement-related limitations were infringed only outside the United States. VLSI Br. 28–36. VLSI argues this conclusion directly

contradicts a pretrial stipulation entered into by the parties, which states:

> Of the total, global number of Intel products and associated activities determined ***(without regard to geographic considerations)*** to meet the technical requirements of any asserted VLSI patent claim not proven invalid by Intel, as well as any actual or projected revenues or profits associated therewith, ***seventy percent (70%) thereof will be deemed to have a United States nexus as required by each subsection of 35 U.S.C. § 271*** and for determining any patent infringement damages in this case. . . . By entering into this agreement, neither party makes any admission about patent infringement or noninfringement, validity or invalidity, or damages.

J.A. 6313 (emphases added). We agree with VLSI.

Interpretation of a "pretrial stipulation, like any contract, presents a legal question" we review de novo. *Kearns v. Chrysler Corp.*, 32 F.3d 1541, 1545 (Fed. Cir. 1994). Here, the stipulation's plain and unambiguous language establishes that, for all accused Intel products and activities determined to meet the technical requirements of the asserted claims, 70% will automatically be treated as having a U.S. nexus for infringement purposes. The district court concluded otherwise, reasoning the stipulation could not establish the requisite U.S. nexus for infringement because "[o]ne of the technical requirements necessary for the nexus to apply is that the claim limitations are met (in the United States)." J.A. 28. This reasoning, however, directly contradicts the stipulation, which requires the technical requirement determination be conducted "*without regard to geographic considerations*." J.A. 6313 (emphasis added). This error warrants reversal.

We are unpersuaded by Intel's arguments that the stipulation merely provided "an agreed-upon accounting

mechanism to simplify the calculation of damages" without addressing the U.S. nexus requirement for infringement. Intel Br. 29; *see also id.* at 27–34. The stipulation, on its face, establishes a U.S. nexus "as required by each subsection of 35 U.S.C. § 271 *and* for determining any patent infringement damages." J.A. 6313 (emphasis added). Section 271 is entirely about infringement, not damages. 35 U.S.C. § 271. Thus, the only reasonable interpretation of the stipulation is that it addresses U.S. nexus for infringement purposes *as well as* for damages calculations.

Intel argues such an "absurd" interpretation would contradict the stipulation's statement that the stipulation was not "any admission about patent infringement." Intel Br. 30–32. But stipulating to a fact relevant to infringement, such as U.S. nexus, is not tantamount to an admission about infringement itself. To prove infringement, VLSI still had to show Intel's accused products and activities met the claims' non-geographic, technical requirements. We see no absurdity in such an attempt to simplify litigation given the stipulation was entered into early in the case when there were eight patents at issue and scores (if not hundreds) of accused products with varying levels of U.S. nexus. Oral Arg. at 2:35–3:03, 32:32–33:55. Even if this strategic choice proved unwise in retrospect, we decline to look past the clear language of the stipulation to "rescue" Intel from its decision to "freely enter[]" an agreement "which it later finds to be imprudently made." *Kearns*, 32 F.3d at 1546.

For the foregoing reasons, we reverse the district court's grant of summary judgment of noninfringement on extraterritoriality grounds for the asserted method claims.

2. The Asserted Apparatus Claims

With respect to the asserted apparatus claims, VLSI argues the district court separately erred in concluding that VLSI cannot prove infringement because it did not provide "evidence that the accused technology is

reasonably capable of meeting the testing claim limitation [(i.e., 'measuring a performance parameter value for a core')] ***in the United States***." VLSI Br. 36–40 (quoting J.A. 29). VLSI argues that it sufficiently showed the accused products corresponded to the patented invention and that they include a "performance measurement circuit for measuring a performance parameter value for said core," as recited in claim 10. *Id.* at 37. In VLSI's view, the district court erred because, despite agreeing the accused devices are reasonably capable of performing the claimed measuring, the court improperly objected to the fact that the measuring was not performed in the United States. *Id.* at 37–38 (citing *Gemtron v. Saint-Gobain Corp.*, 572 F.3d 1371, 1380 (Fed. Cir. 2009)).

Intel reads the district court's order differently, arguing the court was not only concerned with *where* the measuring was performed, but also with whether the accused products alone were *reasonably capable* of "measuring a performance parameter value" without significant alterations. Intel Br. 34–41 (citing *INVT SPE LLC v. Int'l Trade Comm'n*, 46 F.4th 1361, 1375–76 (Fed. Cir. 2022)). According to Intel, the court correctly granted summary judgment of noninfringement because "the only evidence that VLSI presented concerned the alleged capabilities of the accused products when combined with an external testing device called an 'ATE tester' in Intel's overseas manufacturing facilities." *Id.* at 34–35.

We agree with VLSI that the district court erred in granting summary judgment of noninfringement with respect to the asserted apparatus claims. As an initial matter, we believe VLSI has a more reasonable view of the district court's order because Intel's motion for summary judgment focused on *where* the claimed measuring limitations were practiced, not *whether* the accused products were reasonably capable of performing them without significant alterations. *See* J.A. 6196–98 (section titled "Intel is Also Entitled to Summary Judgment of No Infringement

For The '836 Patent Because Intel's Testing Occurs Outside the United States"); *id.* at 6197 (arguing, with respect to the asserted apparatus claims, that "VLSI cannot show that the accused circuity in Intel's products is capable of 'measuring a performance parameter value' *in the United States*" (emphasis added)). Under this view of the district court's order, VLSI is correct that the court improperly focused on where the claimed measuring limitations were practiced instead of the undisputed fact that Intel imported and sold the accused products in the United States. *See Gemtron*, 572 F.3d at 1380 ("[I]t is the infringing act—making, using, offering to sell, selling, or importing—that must be within (or into) the United States.").

We further note that, even under Intel's understanding of the district court's order, there is a genuine dispute of material fact as to whether the accused products are "reasonably capable of performing the claimed functions without significant alterations." *INVT*, 46 F.4th at 1376. The relevant question is not whether Intel's accused products can perform the claimed measuring limitation without assistance from any external device such as an ATE tester. We have previously held that "[w]here . . . a product includes the structural means for performing a claimed function, it can still infringe 'separate and apart' from [an] operating system that is needed to use the product" if it can perform the claimed function without product modification. *Silicon Graphics, Inc. v. ATI Techs., Inc.*, 607 F.3d 784, 794 (Fed. Cir. 2010). The proper inquiry, therefore, is whether Intel's accused products include a performance measurement circuit having "the structural means for performing" the claimed measuring function "without product modification." *See id.* Intel argues that the ATE tester is necessary to perform the "measuring" function. *See* J.A. 8149–50, 200:2–201:1 (discussing use of ATE tester to measure voltage). But VLSI presented evidence raising a genuine dispute as to this issue, including testimony that each core within Intel's accused products has a performance

measurement circuit with dedicated, built-in circuitry for measuring a performance parameter value of that core. *See* J.A. 6247–55 (discussing BISTS [built-in self-tests] and PBISTS [programmable built-in self-tests]). This alone is sufficient to preclude summary judgment of noninfringement, even if we were to accept Intel's reading of the district court's order.

For the foregoing reasons, we reverse the district court's grant of summary judgment of noninfringement on extraterritoriality grounds for the asserted apparatus claims.

B. VLSI's DOE Theory

We turn next to the district court's independent grant of summary judgment that Intel does not infringe the asserted claims of the '836 patent under VLSI's DOE theory. VLSI challenges this conclusion only as it relates to apparatus claim 10 and its dependent claims. VLSI Br. 41. Specifically, VLSI argues the district court incorrectly invoked prosecution disclaimer to construe claim 10 as requiring the claimed "selecting a core" to be performed "*upon identifying*" a single-core task. J.A. 95–98. We agree the court erred in adopting this construction, which was critical to its ultimate grant of summary judgment for the asserted apparatus claims. *See* J.A. 24–26 (rejecting VLSI's DOE theory because it would vitiate the "upon identifying" limitation).

Claim construction is a question of law we review de novo. *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 808 (Fed. Cir. 2021). We review intrinsic-evidence aspects of the court's claim construction analysis de novo and any underlying fact findings about extrinsic evidence for clear error. *Id.* Prosecution history is part of the intrinsic evidence. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (en banc). While we have held that "[a]n applicant's statements to the [Patent Office] characterizing its invention may give rise to prosecution disclaimer," "[t]he doctrine

does not apply unless the disclaimer is 'both clear and unmistakable to one of ordinary skill in the art.'" *Tech. Props. Ltd. LLC v. Huawei Techs. Co.*, 849 F.3d 1349, 1357 (Fed. Cir. 2017) (quoting *Elbex Video, Ltd. v. Sensormatic Elecs. Corp.*, 508 F.3d 1366, 1371 (Fed. Cir. 2007)).

We begin our analysis with the claim language and note that, unlike independent claims 1 and 20, independent claim 10 does not include an "upon identifying" limitation—a fact the district court acknowledged. J.A. 95. The district court nevertheless imported an "upon identifying" limitation into claim 10 because it concluded the patent applicants' statements during prosecution amounted to "clear and unmistakable disavowal of a broader interpretation[.]" J.A. 95–98. We do not agree the statements at issue here are sufficient to meet the high burden for prosecution disclaimer.

The parties primarily dispute the application of our prosecution disclaimer doctrine to three statements made by the patent applicants during prosecution:

1. "Applicants have disclosed and claimed a multi-core system on chip (SoC) and associated method of operation for executing single core jobs or applications on the multi-core SoC by using the actual maximum operating frequencies for the individual cores on the SoC to select which core will execute the single core job/application. To this end, processing speed parameters are measured and stored for each of a plurality of cores, and ***upon identifying*** a single-core processing task that cannot be run by the plurality of cores, the core having the fastest measured processing speed parameter is selected to run the identified single-core processing task. *See, e.g.*, claims 1, 10, and 20." J.A. 1106 (emphasis added).
2. "Instead, the claims require identification of 'a processing task that can not be run by the

> plurality of cores.' *See, e.g.*, claim 1 ('***upon identifying*** a processing task that can not be run by the plurality of cores, selecting a core from the plurality of cores having a fastest measured processing speed parameter to run the processing task') and claim 10 ('a first storage device for storing the performance parameter values for the plurality of cores for use in selecting a core having maximized or minimized performance parameter value to run a processing task that can not be run by the plurality of cores')." J.A. 1107.
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> 3. "Applicants respectfully submit that there is no teaching or suggestion by Kim of identifying tasks 'that can not be run by the plurality of cores,' much less of assigning such single-core tasks to the fastest core, as claimed." J.A. 1107.

None of these statements amounts to a clear and unmistakable disclaimer that claim 10 includes an "upon identifying" limitation. For example, the second and third statements do not connect the words "upon identifying" to claim 10 whatsoever. Moreover, they can reasonably be interpreted as distinguishing the prior art on the basis that claim 10 requires identification of a single-core processing task *irrespective* of when it is done in relation to core selection. We see no clear indication in these statements that the patent applicants intended to limit claim 10 to require core selection to occur only "*upon* identifying" (i.e., *after* identifying) a single-core processing task.

The first statement comes closer to suggesting that claim 10 includes an "upon identifying" limitation requiring a specific order of operations. But even here, the "*see, e.g.*" cite connecting claim 10 to the "upon identifying" language is less than clear. The plain language of claim 10 is broad enough to encompass both (1) embodiments where core selection occurs "upon identifying" a single-core processing task and (2) embodiments where core selection

occurs before or simultaneously to identifying a single-core processing task. Thus, a "*see, e.g.*" cite would be appropriate even *without* limiting the scope of claim 10, and we see no indication the patent applicants intended to make such a limiting disclaimer. Because this statement is, at best, "ambiguous or amenable to multiple reasonable interpretations, prosecution disclaimer is not established." *Tech. Props.*, 849 F.3d at 1358.

In the absence of clear and unmistakable prosecution disclaimer, we conclude the district court erred in construing claim 10 to include an unrecited "upon identifying" limitation. We accordingly reverse the court's resulting grant of summary judgment that Intel does not infringe claim 10 and its dependent claims under VLSI's DOE theory.[2]

II. Striking of Dr. Sullivan's Damages Theories

We now consider the district court's striking of Dr. Sullivan's damages theories due to VLSI's purported failure to adequately disclose them in accordance with the court's local patent rules.

We review a district court's application of local patent rules for abuse of discretion. *Keranos, LLC v. Silicon Storage Tech., Inc.*, 797 F.3d 1025, 1035 (Fed. Cir. 2015). A district court abuses its discretion when "(1) the decision was clearly unreasonable, arbitrary, or fanciful; (2) the decision was based on an erroneous conclusion of law; (3) the court's findings were clearly erroneous; or (4) the record contains no evidence upon which the court rationally could have based its decision." *Id.* The Northern District of California's Patent Local Rule 3-8 requires the plaintiff to disclose its "theories of recovery, factual support for those theories, and [exemplary] computation of damages." P.L.R.

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[2] We leave undisturbed the court's DOE-related grant of summary judgment with respect to the remaining asserted claims, which were not challenged on appeal.

3-8 (eff. Jan. 17, 2017). It "does not require certainty and is not fairly interpreted as replacing the robust analysis of a patent damages expert report." *Twilio, Inc. v. Telesign Corp.*, No. 16-cv-06925, 2017 WL 5525929, at *2 (N.D. Cal. Nov. 17, 2017).

A magistrate judge for the district court struck Dr. Sullivan's damages theories that relied on net present value (NPV) and value per unit (VPU) methods for estimating a reasonable royalty because he concluded Dr. Sullivan's expert report exceeded what was disclosed in VLSI's damages contentions in violation of Patent Local Rule 3-8. J.A. 71–73 (order); J.A. 2153–377 (damages contentions). The order criticized VLSI's contentions for their "scattershot references to Intel data or documents," noting that "[s]uch vague and imprecise citations to internal documents and analyses does not give Intel notice of VLSI's theory and promotes the 'type of inferential guesswork . . . [the] damages contentions are intended to avoid.'" J.A. 72 (citing *Looksmart Grp., Inc. v. Microsoft Corp.*, 386 F. Supp. 3d 1222, 1234 (N.D. Cal. 2019)). A separate district court judge then denied VLSI's motion to reverse the order striking Dr. Sullivan's testimony, finding no clear error in the magistrate judge's determinations that VLSI did not properly disclose the data underlying Dr. Sullivan's NPV and VPU theories. J.A. 58–65.

We identify no abuse of discretion in the magistrate judge's application of the court's local patent rules in striking Dr. Sullivan's damages theories. Nor do we identify an abuse of discretion in the district judge's subsequent order confirming the same. Without opining on the precise contours of Patent Local Rule 3-8, we conclude it was not clearly erroneous for the district court to find that the limited support relied on by VLSI in its damages contentions, the disparate placement of relevant references (including in several-page-long string citations), and the failure to expressly disclose readily available figures later relied on by Dr. Sullivan were insufficient to notify Intel of the data

underlying Dr. Sullivan's NPV and VPU theories. *See* J.A. 72–73; J.A. 61–64. This is especially true in the context of this litigation, where (1) VLSI's damages contentions had become a "recurring issue between the parties," J.A. 66–67, and (2) the court had previously warned VLSI that its damages contentions must "describe with specificity the bases for its damages claim" including "[a]n identification and explanation of each specific damages theory that VLSI intends to pursue," "[a]ll facts known to VLSI that support each such damages theory," and "[a]ll calculations known to VLSI on which VLSI bases each such damages theory," J.A. 8075.

We note that while the district court did not abuse its discretion in striking Dr. Sullivan's NPV and VPU damages theories, it left untouched the damages theories of another VLSI expert, Mr. Chandler. J.A. 68–69. VLSI thus maintains the ability to prove damages based on Mr. Chandler's opinions and can do so on remand.

CONCLUSION

We have considered the parties' remaining arguments and find them unpersuasive. For the foregoing reasons, we (1) reverse the district court's grant of summary judgment of noninfringement of the '836 patent on extraterritoriality grounds, (2) reverse the court's grant of summary judgment based on the rejection of VLSI's DOE theory as it relates to the asserted apparatus claims (claims 10, 11, 13, and 17), and (3) affirm the court's striking of Dr. Sullivan's NPV and VPU damages theories. We remand for further proceedings consistent with this opinion.

REVERSED-IN-PART, AFFIRMED-IN-PART, AND REMANDED

COSTS

No costs.