NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

KATANA SILICON TECHNOLOGIES LLC,
Appellant

v.

MICRON TECHNOLOGY, INC.,
Appellee

2024-2100, 2024-2101, 2024-2103

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2023-00071, IPR2023-00072, IPR2023-00073.

Decided: April 21, 2026

HOWARD LITHAW LIM, Carter Arnett PLLC, Dallas, TX, argued for appellant. Also represented by SCOTT W. BREEDLOVE.

ANDREW DUFRESNE, Perkins Coie LLP, Madison, WI, argued for appellee. Also represented by AMANDA TESSAR, Denver, CO; AMY ELIZABETH SIMPSON, Holland & Knight LLP, Los Angeles, CA.

Before TARANTO, CLEVENGER, and STOLL, *Circuit Judges*.

STOLL, *Circuit Judge*.

Katana Silicon Technologies LLC appeals from three final written decisions of the United States Patent and Trademark Office Patent Trial and Appeal Board in *inter partes* reviews of U.S. Patent Nos. RE38,806 and 6,352,879. In its final written decisions, the Board held claims 1–33 of the '806 patent and claims 1–15 of the '879 patent unpatentable as obvious under 35 U.S.C. § 103. In making that determination, the Board adopted a claim construction Katana challenges on appeal. Because we adopt the Board's construction, we affirm the Board's decisions.

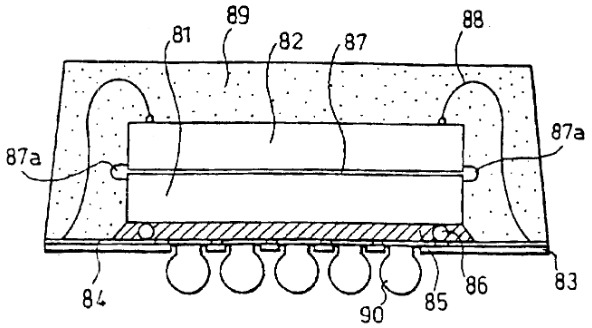
BACKGROUND

The '806 and '879 patents disclose "a semiconductor device having a structure substantially miniaturized to a chip size, i.e., a CSP (Chip Size Package) structure, and a method of manufacturing such a semiconductor device." U.S. Patent No. RE38,806 col. 1 ll. 17–20.[1] The patents specifically describe a miniaturized semiconductor device having a CSP that includes multiple semiconductor chips stacked vertically inside the package (i.e., a stacked package structure). *Id.* at col. 1 ll. 15–20, col. 1 ll. 53–65, col. 2 ll. 63–65. For example, Figure 14(a) of the '806 patent (reproduced below) shows a cross-sectional view of a

[1] The '806 and '879 patents have identical specifications except for their respective priority statements and an explanation of markup notations unique to the reissued '806 patent. *Compare* '806 patent col. 1 ll. 4–12, *with* U.S. Patent No. 6,352,879 col. 1 ll. 4–7. Because the patents share a common specification, we refer only to the '806 patent specification unless otherwise specified.

conventional semiconductor device having a stacked package structure. *Id.* at col. 6 ll. 24–26.

FIG.14(a)



Id. Fig. 14(a). The specification explains that in a conventional semiconductor device where multiple semiconductor chips are stacked and laminated, two different methods are used to bond the laminated semiconductor chips to each other—"an adhesive agent (paste) potting method and a method using a thermo-compression sheet." *Id.* at col. 2 ll. 16–22.

In the potting method, if the amount of the adhesive agent is excessive, the adhesive agent may spread and overflow beyond the outer edge of the semiconductor chips, as illustrated by overflown adhesive agent 87a between semiconductor chips 81 and 82 in Figure 14(a). *Id.* at col. 2 ll. 23–29. Such overflown adhesive agent may contact wires in the package or the electrode pad of the semiconductor chips, so the wiring must be provided far from the side surfaces of the chips, which increases the package size. *Id.* at col. 2 ll. 30–43. "On the other hand, if the amount of the adhesive agent is too small, a gap is produced between the semiconductor chips 81 and 82 . . . causing problems such as separation of the semiconductor chip 82 from the semiconductor chip 81." *Id.* at col. 2 ll. 44–48.

In the method using a thermo-compression sheet, the thermo-compression sheet is disposed on the surface of a first semiconductor chip, and then a second semiconductor

chip is adhered to the thermo-compression sheet. *Id.* at col. 2 ll. 49–56, col. 4 ll. 12–22, col. 9 ll. 46–50. Thus, the thermo-compression sheet must be the same size as semiconductor chip 82 and must be placed accurately at a specific location on semiconductor chip 81. *Id.* at col. 2 ll. 49–53. "In addition, the semiconductor chip 82 must be bonded to the thermo-compression sheet so as to be located exactly on the top of the thermo-compression sheet." *Id.* at col. 2 ll. 53–57. This process thus requires accurate positioning twice, "i.e., positioning the thermo-compression sheet, etc., and positioning the first or second semiconductor chip on the thermo-compression sheet." *Id.* at col. 3 ll. 33–38.

The '806 and '879 patents purport to avoid these complications with the conventional bonding methods by forming an "adhesion layer" "in advance" on a back surface of a wafer that has a circuit formed on its front surface. *Id.* at col. 4 ll. 17–20, col. 6 ll. 42–45. In other words, the adhesion layer is formed on a wafer during the semiconductor fabrication process before the wafer is cut or diced to produce individual chips with adhesion layers. *Id.* at col. 4 ll. 17–63. By applying the adhesion layer in advance, "the adhesive agent does not overflow the space between the first and second semiconductor chips," which allows other components like wiring to be positioned closer to the chip edges and allows the chip to be mounted "by accurately positioning it once." *Id.* at col. 4 ll. 57–63, col. 5 ll. 15–29, col. 3 ll. 19–44, col. 3 l. 66–col. 4 l. 24, col. 4 ll. 48–56.

Every independent claim of the '806 and '879 patents requires at least one "adhesion layer" on the back surface of a chip for mounting the chip in a stack. For example, claim 1 of the '806 patent recites:

> 1. A semiconductor device including a stacked package structure and a chip size package structure, comprising:

> an insulating substrate including a wiring layer having electrode sections;
>
> a first semiconductor chip having *a first adhesion layer* adhered to its back surface where a circuit is not formed, said first semiconductor chip being mounted on said wiring layer through the first adhesion layer; and
>
> a second semiconductor chip having *a second adhesion layer* adhered to its back surface where a circuit is not formed, said second semiconductor chip being mounted on a circuit-formed front surface of said first semiconductor chip through the second adhesion layer;
>
> each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire, said first and second semiconductor chips and the wire being sealed with a resin.

Id. at col. 13 ll. 45–63 (emphases added).

Micron Technology, Inc. filed three petitions for *inter partes* review, arguing that International Patent Application Publication No. WO 96/13066 ("Mostafazadeh"), in combination with other references not pertinent to this appeal, rendered all claims of the '806 and '879 patents obvious. Mostafazadeh, like the '806 and '879 patents, recognizes the advantages of forming a layer that provides adhesion on a wafer before the wafer is cut or diced to produce individual chips with adhesive layers that neither overflow nor underfill the chip's surface. *See* J.A. 1280–83. Most relevant to Katana's arguments on appeal, Mostafazadeh's adhesive layer is formed on the wafer, dried, diced, and later cured during bonding. J.A. 1282, 1284–85, 1297.

The Board held all the challenged claims obvious under § 103 in view of Mostafazadeh, in combination with other

references. The Board construed the term "adhesion layer" to not be limited to a *pre-formed* solid sheet, such as a thermo-compression sheet. *See, e.g.*, J.A. 21–22. Instead, the Board rejected Katana's proposal to construe the term as "a pre-formed layer that is adhered" and adopted Micron's proposed construction—"a layer that adheres." J.A. 16–26. The Board reasoned that several claims and the shared specification expressly called for "forming" an adhesion layer on the back surface of a wafer, which it viewed as strongly suggesting that an "adhesion layer" need not always be "pre-formed." Rather, the Board reasoned, the adhesion layer could "be formed *in situ* on the back surface of a wafer." J.A. 18–21. And rather than finding the specification's use of a thermo-compression sheet in both preferred embodiments to be definitional or critical to the goal of avoiding overflow or underfill, the Board concluded that the specification described drawbacks of using adhesives *and* thermo-compression sheets and that the disclosed solution to both sets of issues was in forming an adhesion layer at the wafer stage before the wafer is diced into individual chips. J.A. 22, 25–26.

Katana timely appealed. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

"Claim construction is a question of law with underlying questions of fact." *Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1278 (Fed. Cir. 2017). Where "the intrinsic record fully governs the proper construction of a term," our review is de novo. *Id.*

The sole dispute in this appeal is whether the Board erred in construing the claim term "adhesion layer" as "a layer that adheres." Katana insists that the adhesion layer must be "a pre-formed layer that is adhered," such that the adhesion layer is a solid sheet disposed in advance on the wafer before the wafer is diced and cannot be formed from an adhesive that is later cured, as in Mostafazadeh.

Micron, by contrast, defends the Board's view, which is that neither the claims nor the specification requires a pre-formed solid sheet to avoid adhesive potentially overflowing or underfilling the space between a chip's surface and the mounting surface. We agree with the Board.

Looking first at the claim language, the term "adhesion layer" merely requires a layer that provides adhesion. That is, "adhesion" is an adjective modifying the noun "layer" to specify the type or purpose of the layer. Nothing in the claim language requires a fully-formed or "pre-formed" adhesion layer where no further processing is required. *See, e.g.*, '806 patent col. 13 ll. 45–63. Had the patentee intended to limit the claims to a pre-formed adhesion layer with no further required processing, it could have included language in the claims to that effect.

Katana argues that claim 30 of the '806 patent requires "forming" the first and second adhesion layers on a back surface of the wafers before producing separate chips from those wafers by dicing and mounting the chips in a stack. According to Katana, these limitations exclude an adhesion layer that is not fully pre-formed in advance. However, Katana never asked for a construction of "forming," so we must apply the ordinary meaning of the plain claim language. And while the ordinary meaning of "forming a first insulating adhesion layer" includes adhesion layers that are pre-formed, it does not in fact exclude forming an adhesion layer on a wafer and curing it after dicing. *See id.* at col. 17 l. 58–col. 18 l. 17. Indeed, nowhere does claim 30 exclude using an adhesive agent, such as a glue or paste that is later cured, to form an adhesion layer. Thus, the Board's construction is consistent with the plain claim language.

The Board's construction is also more consistent with the specification than Katana's. Although both preferred embodiments described in the specification disclose a pre-formed thermo-compression sheet as an adhesion layer,

"[t]here is a fine line between reading the claims in light of the specification and importing limitations from the specification into the claims." *IQRIS Techs. LLC v. Point Blank Enters., Inc.*, 130 F.4th 998, 1003–04 (Fed. Cir. 2025). Here, where there is no evidence suggesting that the ordinary meaning of adhesion layer is limited to a thermo-compression sheet or even to a fully pre-formed layer, "we are not inclined to import limitations from the preferred embodiments into the claimed invention." *Id.* at 1004 (citing *Playtex Prods., Inc. v. Procter & Gamble Co.*, 400 F.3d 901, 907–08 (Fed. Cir. 2005) (collecting cases)).

Moreover, "[a]bsent lexicography or disavowal, we do not depart from the plain meaning of the claims." *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016). Contrary to Katana's assertion, there is no clear disavowal of using adhesive agents such as glue or paste to form an adhesion layer or lexicography that would exclude such an adhesion layer in the specification or prosecution history. The specification does not limit an adhesion layer to a thermo-compression sheet but instead discloses a thermo-compression sheet as an example of an adhesion layer. For example, a first embodiment, described as simply "one embodiment of the present invention," includes a chip mounted "through a thermo-compression sheet (adhesion layer) 6 so that its back surface is adhered to the thermo-compression sheet 6." '806 patent at col. 6 ll. 34–35, col. 6 ll. 48–52. Similarly, in a second embodiment, "[t]he thermo-compression sheet 6 is provided *as an adhesion layer* for holding" a first chip on a second chip. *Id.* at col. 11 ll. 31–33 (emphasis added). In both instances, we read the specification's use of the term "adhesion layer" as referring to the role of the thermo-compression sheet in the device, not as defining "adhesion layer" as a thermo-compression sheet. Although the specification includes only these two exemplary embodiments, "[w]e have cautioned against reading limitations into a claim from the preferred embodiment described in the

specification, even if it is the only embodiment described, absent clear disclaimer in the specification." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004). And when we read these embodiments in light of the rest of the specification, we are not convinced that these exemplary embodiments represent clear disclaimer of other types of adhesion layers.

Indeed, although Katana argues that the specification consistently uses the term "adhesive agent" to refer to glue or paste and the term "adhesion layer" to refer to solid, preformed layers, *see* Appellant's Reply Br. 11–12, the specification makes clear that an adhesion layer can be formed from an adhesive agent because it uses these terms interchangeably. For example, after describing a method of manufacturing a semiconductor device using a first and second "*adhesion layer*," the specification states, "in the above manufacturing method, the *adhesive agent* does not overflow the space between the first and second semiconductor chips." '806 patent at col. 4 ll. 57–62, col. 4 ll. 25–47 (emphasis added); *id.* at col. 5 ll. 23–28, col. 4 l. 64–col. 5 l. 14. Katana argues that "[t]he phrase 'the adhesive agent,'" as it is used in this context "actually refers back to the 'an adhesive agent' in the problem description in the background of the invention section," and concludes that "the phrase 'the adhesive agent' more likely means that the problem . . . is solved by the manufacturing method and not that the manufacturing method contemplates using an adhesive agent." Appellant's Br. 45–46. But the more consistent reading of the specification is that the manufacturing method of forming the adhesion layer at the wafer stage solves the problems described in the specification even when using an adhesive agent that later becomes an adhesion layer.

Indeed, the specification explains that its manufacturing methods of forming the adhesion layers "in advance" on the back of wafers before dicing avoids the issue of overflow, which leads to a smaller package size, and provides

the benefits of requiring only one positioning step and a simplified manufacturing process. *See* '806 patent at col. 4 ll. 48–62, col. 4 ll. 17–24, col. 5 ll. 15–29, col. 3 ll. 37–44. Thus, given the claim language, the absence of lexicography or disavowal, and the specification's described solutions to the problems of conventional devices and methods of manufacture, we do not adopt Katana's interpretation requiring an adhesion layer to be a pre-formed layer.

Although Katana argues that its factual attacks on the prior art and obviousness combinations proposed by Micron do not depend on any claim construction, Katana's own statements contradict this argument. Appellant's Reply Br. 9, 22. For example, Katana contends that "even under the Board's faulty construction, Mostafazadeh still does not disclose the claimed adhesion layer and render the claims obvious because its process would not *fully form* the purported adhesion layer on the wafer but instead on the chips after mounting." Appellant's Reply Br. 9 (emphasis added). Because we adopt the Board's contrary construction that does not require a pre-formed layer, we are not persuaded.

CONCLUSION

We have considered Katana's remaining arguments and find them unpersuasive. For the foregoing reasons, we affirm the Board's final written decisions in all three proceedings.

AFFIRMED